IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered). Please AMEND claims 1, 8, 14-18, and 39 in accordance with the following:

1. (CURRENTLY AMENDED) A differential signal output apparatus comprising:

a first differential pair ~~for~~ receiving differential signals, said first differential pair having~~,~~ first transistors;

a first current source, connected to one end of the first differential pair at a first branching node branching current from the first current source to the first transistors;

a second differential pair receiving the differential signals, said second differential pair having second transistors;

a second current source connected to one end of the second differential pair at a second branching node branching current from the second current source to the second transistors; and

a capacitor, ~~connected~~ provided between the first branching node and the second branching node, and being directly connected to the first branching node and the second branching node ~~so that the capacitor, the first current source, and the second current source are connected in series~~.

2. (PREVIOUSLY PRESENTED) The differential signal output apparatus, as claimed in Claim 1, wherein:

the capacitor, the first current source, and the second current source are connected between a first low impedance node and a second low impedance node.

Claims 3 - 5 (CANCELED)

6. (PREVIOUSLY PRESENTED) The differential signal output apparatus, as claimed in Claim 1, wherein:

the capacitor forms a current path allowing the current supplied from one of the first and second current sources to flow when the current to one of the first and second differential pair is

cut off.

7. (CANCELED)

8. (CURRENTLY AMENDED) A differential signal output apparatus comprising:

a first differential pair receiving differential signals, said first differential pair having first transistors;

a first current source, connected to one end of the first differential pair at a first branching node branching current from the first current source to the first transistors;

a second differential pair receiving the differential signals, said second differential pair having second transistors;

a second current source connected to one end of the second differential pair at a second branching node branching current from the second current source to the second transistors; and

a transitional response circuit forming a current path allowing ~~one of~~ the current supplied from one of the first and second current sources to flow when the current to one of the first and second differential pair is cut off.

9. (ORIGINAL) The differential signal output apparatus, as claimed in Claim 8, wherein:

the transitional response circuit is a capacitor.

10. (ORIGINAL) The differential signal output apparatus, as claimed in Claim 6, wherein:

the impedance of the capacitor is smaller than the load impedance in the differential signal output apparatus at a transitional response frequency at which a transitional current flows to the capacitor.

11. (CANCELED)

12. (ORIGINAL) The differential signal output apparatus, as claimed in Claim 9, wherein:

the impedance of the capacitor is smaller than the load impedance in the differential signal output apparatus at a transitional response frequency at which a transitional current flows to the capacitor.

13. (CURRENTLY AMENDED) A semiconductor integrated circuit apparatus provided with a differential output circuit comprising:

a first differential pair constituted by arranging wiring between differential input signals and differential output signals arranging first transistors symmetrically;

a first current source connected to one end of the first differential pair so arranged that first connection wiring lines to the first transistors be symmetrical; and

a second differential pair constituted by arranging wiring between the differential input signals and the differential output signals arranging second transistors symmetrically;

a second current source connected to one end of the second differential pair so arranged that second connection wiring lines to the second transistors be symmetrical; and

a capacitor, ~~connected~~ provided between a first branching node and a second branching node for the first and second connection wiring lines from the first current source and the second current source to the first and second transistors, and directly connected to the first branching node and the second branching node ~~arranged in an area between the first and second transistors~~.

14. (CURRENTLY AMENDED) A semiconductor integrated circuit apparatus provided with a differential output circuit comprising:

a first differential pair constituted by arranging wiring between differential input signals and differential output signals arranging first transistors symmetrically;

a first current source connected to one end of the first differential pair so arranged that first connection wiring lines to the first transistors be symmetrical;

a second differential pair constituted by arranging wiring between the differential input signals and the differential output signals arranging second transistors symmetrically;

a second current source connected to one end of the second differential pair so arranged that second connection wiring lines to the second transistors be symmetrical~~symmetrically~~; and

a capacitor, ~~connected~~ provided between a first branching node and a second branching node for the first and second connection wiring lines from the first current source and the second current source to the first and second transistors, and directly connected to the first branching node and the second branching node ~~arranged in an area between the first and second transistors~~,

wherein a current supply ability of the second current source is same as or greater than a

current supply ability of the first current source.

15. (CURRENTLY AMENDED) A semiconductor integrated circuit apparatus provided with a

differential output circuit comprising:

a first differential pair constituted by arranging wiring between differential input signals and between differential output signals and arranging transistors of a first conductivity type symmetrically;

a first current source connected to one end of the first differential pair and so arranged that connection wiring lines to the transistors of the first conductivity type be symmetrical;

a second differential pair arranged opposite to the first differential pair, constituted by arranging wiring between differential input signals and between differential output signals and arranging transistors of a second conductivity type symmetrically;

a second current source connected to one end of the second differential pair and so arranged that connection wiring lines to the transistors of the second conductivity type be symmetrical; and

a capacitor, ~~connected~~ provided between a first branching node for branching connection wiring from the first current source to the transistors of the first conductivity type and a second branching node for branching connection wiring from the second current source to the transistors of the second conductivity type, and directly connected to the first branching node and the second branching node ~~arranged in an area surrounded by the first differential pair and the second differential pair~~.

16. (CURRENTLY AMENDED) A differential signal transmission system provided with a differential output circuit, the differential output circuit comprising:

a first differential input unit into which differential signals are entered;

a first current supply unit supplying a current to the first differential input unit;

a second differential input unit into which the differential signals are entered;

a second current supply unit supplying a current to the second differential input unit; and

a capacitor, ~~connected~~ provided between a first connection node between the first differential input unit and the first current supply unit and a second connection node between the second differential input unit and the second current supply unit, and being directly connected to the first branching node and the second branching node ~~so that the capacitor, the first current~~

~~supply unit, and the second current supply unit are connected in series~~.

17. (CURRENTLY AMENDED) A differential signal transmission system provided with a differential output circuit, the differential output circuit comprising:

a first differential input unit into which differential signals are entered;

a first current supply unit supplying a current to the first differential input unit;

a second differential input unit into which the differential signals are entered;

a second current supply unit supplying a current to the second differential input unit; and

a capacitor, ~~connected~~ provided between a first connection node and a second connection node, which is directly connected to the first branching node and the second branching node, and the first and second connection nodes respectively connecting the first current supply unit to the first differential input unit and the second current supply unit to the second differential input unit,

wherein a current supply ability of the second current supply unit is same as or greater than a current supply ability of the first current supply unit.

18. (CURRENTLY AMENDED) A differential signal transmission system provided with a differential output circuit, the differential signal transmission system comprising:

a first differential input unit configured in a first conductivity type entering differential signals;

a first current supply unit supplying a current to the first differential input unit;

a second differential input unit configured in a second conductivity type, of which differential output terminals are connected to differential output terminals of the first differential input unit to receive the differential signals;

a second current supply unit supplying a current to the second differential input unit; and

a capacitor, ~~connected~~ provided between a connection node between the first differential input unit and the first current supply unit and another connection node between the second differential input unit and the second current supply unit, and being directly connected to the connection node and the another connection node.

Claims 19 - 38 (CANCELED)

39. (CURRENTLY AMENDED) A differential signal output apparatus comprising:

a first differential pair to receive differential signals;

a first current source connected to the first differential pair at a first branching node;

a second differential pair to receive the differential signals~~singles~~;

a second current source connected to the second differential pair at a second branching node; and

a capacitor, ~~connected~~ provided between the first branching node and the second branching node, and being directly connected to the first branching node and the second branching node ~~to connect the capacitor, the first current source, and the second current source in series~~.